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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/624,438	07/24/2000	Xiaopin Zhang	GR 99 P 2378	5408

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EXAMINER

NGUYEN, LINH M

ART UNIT

PAPER NUMBER

2816

DATE MAILED: 06/19/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/624,438

Applicant(s)

ZHANG ET AL.

Examiner

Linh M. Nguyen

Art Unit

2816

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 24 July 2000.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 11-21 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 11-21 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 24 July 2000 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 9,10,11.
- 4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other:

DETAILED ACTION

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Inventorship

2. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Drawings

3. The drawings are objected to because all the blank boxes [6, 7, 9, 10] in figure 1 are not filled in with corresponding parameters.

To clarify the claimed invention, all the boxes [6, 7, 9, 10] in figure 1 should be filled in with the corresponding parameters, ie. PLL in box 6, etc..

Correction is required. See 37 CFR 1.84(o).

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Abstract objection

4. The abstract of the disclosure is objected to because of an existing space between lines 2 and 4.

Correction is required. See MPEP § 608.01(b).

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 11-17 are rejected under 35 U.S.C. 102(b) as being anticipated by Chonan (U.S. Patent No. 5,463,588).

With respect to claim 11, Chonan discloses, in Figure 1, a controllable current source circuit comprising 1) an output [VINT], 2) supply voltage terminals [VCC, GROUND], and 3) first and second driver stages [2, 1] connected in series between the voltage supply terminals and having a mutual junction point [connection between points at the sources of transistors 12 and 22] connected to the output [VINT]; wherein only the first driver stage switches on and off in dependence on an input signal [ϕ_0], and the second driver stage is switched on and carries a stabilized current.

With respect to claim 12, Chonan discloses, in Figure 1, that the first driver stage forms a part of a current mirror circuit [21] receiving a flow of a stabilized current when the first driver stage is switched on.

With respect to claim 13, Chonan discloses, in Figure 1, that the second driver stage forms a part of a current mirror circuit [11] causing a constant stabilized current to flow in the second driver stage.

With respect to claim 14, Chonan discloses, in Figure 1, that the current mirror circuit [11] is coupled to a current mirror circuit [21] connected to the first driver stage and causes a stabilized current to flow in the current mirror circuit connected to the first driver stage.

With respect to claims 15 and 16, Chonan discloses, in Figures 1 and 2, that a current [I2] carried by the first driver stage [2] when the first driver stage is switched on is *greater/multiple times greater* than a current carried by the second driver stage [I1].

With respect to claim 17, Chonan discloses, in figure 2, that the current I2 carried in the first driver stage is four times greater than the current I1 carried by the second driver stage.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

8. Claims 18, 19, and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chonan (U.S. Patent No. 5,463,588) in view of Olgaard et al. (U.S. Patent No. 5,939,949).

With respect to claims 18, 19, and 21, Chonan discloses, in Figure 1, all the claimed limitations as expressly recited in claim 1, except for a phase locked loop which comprises: 1) a phase comparator having a phase comparison circuit a) with a reference signal input for receiving a reference signal and an input for receiving an input signal whose phase angle is to be

regulated, and b) connected to the current mirror for stabilizing a current flowing into the comparison circuit and into the second driver circuit, 2) a loop filter having an output for outputting an output signal controlling the phase angle of the input signal, and 3) a comparator configured to switch between two output states and having a single output terminal connected to the current source.

Olgaard et al., discloses, in Figs. 1 and 4, a phase locked loop circuit comprising (1) a phase comparator [103] having a phase comparison circuit (a) with a reference signal input [R_SIG] for receiving a reference signal, and an input [N_SIG] for receiving an input signal whose phase angle is to be regulated, and b) connected to a current mirror [404] for stabilizing a current flowing into the comparison circuit and into a second driver circuit [403, 405, 407], 2) a loop filter [107], 3) a comparator [103] being configured to switch between two output states and having a single output terminal connected to the current source [105,106].

To modify the device of Chonan by additionally configuring a phase locked loop circuit comprising 1) a phase comparator having a phase comparison circuit a) with a reference signal input for receiving a reference signal and an input for receiving an input signal whose phase angle is to be regulated, and b) connected to the current mirror for stabilizing a current flowing into the comparison circuit and into the second driver circuit, 2) a loop filter having an output for outputting an output signal controlling the phase angle of the input signal, and 3) a comparator configured to switch between two output states and having a single output terminal connected to the current source, for maximal synchronization and reduced power consumption would have been obvious to one of ordinary skills in the art at the time of the invention since such a

configuration of the phase locked loop with specifically detailed connections has been well-known in the art as evidenced by the teachings of Olgard et al..

9. Claim 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chonan (U.S. Patent No. 5,463,588) in view of Olgaard et al. (U.S. Patent No. 5,939,949), as applied in claim 18, and further in view of Tomassetti et al. (U.S. Patent No. 5,043,677).

With respect to claim 20, the combination Chonan and Olgaard et al. disclose all of the limitations, as indicated in claim 18, except for an exclusive-OR gate being included in the phase comparison circuit. Tomassetti et al. discloses, in Fig. 1, a phase locked loop system comprising a comparator [16] having an exclusive-OR gate [16]. To include an exclusive-OR gate in the phase comparison circuit of the combination Chonan and Olgaard et al. to facilitate the system with high sensitivity to phase error would have been obvious to one of ordinary skills in the art at the time of the invention since such a configuration of an exclusive-OR gate in the phase comparison circuit has been a well-known practice in the art as evidenced by the teachings of Tomassetti et al..

Inquiry

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Linh M. Nguyen whose telephone number is (703) 305-0414. The examiner can normally be reached on Alternate Mon, Tuesday - Friday from 7:30 to 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on (703) 308-4876. The fax phone numbers for the

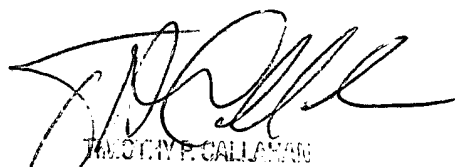
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organization where this application or proceeding is assigned are (703) 872-9318 for regular communications and (703) 872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Linh M. Nguyen



TIMOTHY P. CALLAHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800